We claim:

1. An apparatus, comprising:
write cache storage to store cache lines of write data;
a flush dispatcher coupled to the write cache storage to dispatch the cache lines to memory;
control logic to:
select a first cache line with a first address in the write cache storage for dispatching;
determine if a second cache line in the write cache storage has a second address within a predetermined range of the first address; and
dispatch the first and second cache lines if the second address is within the predetermined range of the first address.

2. The apparatus of claim 1, wherein the predetermined range is programmable.

3. The apparatus of claim 1, wherein control logic to select a first cache line includes logic to select an oldest cache line in the write cache storage.

4. A method, comprising:
receiving a plurality of write requests and storing the plurality of write requests in a plurality of cache lines in a write cache storage;
selecting a first one of the plurality of cache lines for dispatching to a memory, wherein the first one of the plurality of cache lines has a first address;

determining if a second one of the plurality of cache lines has a second address within a predetermined range of the first address;

dispatching the first and second ones of the plurality of cache lines to the memory if the second address is within the predetermined range of the first address; and

dispatching the first one but not the second one of the plurality of cache lines to the memory if the second address is not within the predetermined range of the first address.

5. The method of claim 4, wherein selecting a first one includes selecting an oldest of the plurality of cache lines.

6. The method of claim 4, further comprising programming the predetermined range before selecting.

7. A machine-readable medium having stored thereon instructions, which when executed by a processor cause said processor to perform:

receiving a plurality of write requests and storing the plurality of write requests in a plurality of cache lines in a write cache storage;

selecting a first one of the plurality of cache lines for dispatching to a memory, wherein the first one of the plurality of cache lines has a first address;

determining if a second one of the plurality of cache lines has a second address within a predetermined range of the first address;

dispatching the first and second ones of the plurality of cache lines to the memory if the first address is within the predetermined range of the second address; and

dispatching the first one but not the second one of the plurality of cache lines to the memory if the second address is not within the predetermined range of the first address.

8. The medium of claim 7, wherein selecting a first one includes selecting an oldest of the plurality of cache lines.

9. The medium of claim 7, further comprising programming the predetermined range before selecting.

10. An apparatus, comprising:

write cache storage to store cache lines of write data;

a flush dispatcher coupled to the write cache storage to dispatch the cache lines to memory;

control logic to:

dispatch at least one of the cache lines to memory if the number of cache lines in the write cache storage exceeds a first predetermined value; and

not dispatch any of the cache lines to memory if the number of cache lines in the write cache storage does not exceed the first predetermined value.

11. The apparatus of claim 10, wherein the control logic is further to:

dispatch the at least one of the cache lines with a high priority if the number of cache lines in the write cache storage exceeds a second predetermined value higher than the first predetermined value; and

dispatch the at least one of the cache lines with a low priority if the number of cache lines in the write cache storage does not exceed the second predetermined value.

12. The apparatus of claim 10, wherein the control logic is further to dispatch an oldest one of the cache lines first if the number of cache lines in the write cache storage exceeds the first predetermined value.

13. A method, comprising:

storing write requests in cache lines of write data in write cache storage;

dispatching at least one of the cache lines to memory if the number of cache lines in the write cache storage exceeds a first predetermined value; and

not dispatching any of the cache lines to memory if the number of cache lines in the write cache storage does not exceed the first predetermined value.

14. The method of claim 13, wherein dispatching further includes:

dispatching the at least one of the cache lines with a high priority if the number of cache lines in the write cache storage exceeds a second predetermined value higher than the first predetermined value; and

dispatching the at least one of the cache lines with a low priority if the number of cache lines in the write cache storage does not exceed the second predetermined value.

15. The method of claim 13, wherein dispatching further includes dispatching an oldest one of the cache lines first if the number of cache lines in the write cache storage exceeds the first predetermined value.

16. A machine-readable medium having stored thereon instructions, which when executed by a processor cause said processor to perform:

storing write requests in cache lines of write data in write cache storage;

dispatching at least one of the cache lines to memory if the number of cache lines in the write cache storage exceeds a first predetermined value; and

not dispatching any of the cache lines to memory if the number of cache lines in the write cache storage does not exceed the first predetermined value.

17. The medium of claim 16, wherein dispatching further includes:

dispatching the at least one of the cache lines with a high priority if the number of cache lines in the write cache storage exceeds a second predetermined value higher than the first predetermined value; and

dispatching the at least one of the cache lines with a low priority if the number of cache lines in the write cache storage does not exceed the second predetermined value.

18. The medium of claim 16, wherein dispatching further includes dispatching an oldest one of the cache lines first if the number of cache lines in the write cache storage exceeds the first predetermined value.

19. An apparatus, comprising:

write cache storage to receive a plurality of partial write requests for merging into associated cache lines of write data;

a flush dispatcher coupled to the write cache storage to dispatch the cache lines to memory;

control logic to:

determine if a first cache line associated with a first of the plurality of partial write requests is stored in the write cache storage;

if the first cache line is not stored in the write cache storage:

retrieve the first cache line from memory;

store the retrieved first cache line in the write cache storage; and

merge the first of the plurality of partial write requests into the retrieved first cache line.

20. The apparatus of claim 19, wherein the control logic is further to merge a second of the plurality of partial write requests into the retrieved first cache line if the retrieved first cache line is associated with the second of the plurality of partial write requests.

21. The apparatus of claim 19, wherein the control logic is further to merge the first of the plurality of partial write requests into the first cache line if the first cache line is determined to be stored in the write cache storage.

22. A method, comprising:

receiving a plurality of partial write requests for merging into associated cache lines of write data in write cache storage;

determining if a first cache line associated with a first of the plurality of partial write requests is stored in the write cache storage; and

if the first cache line is not stored in the write cache storage:

retrieving the first cache line from memory;

storing the retrieved first cache line in the write cache storage; and

merging the first of the plurality of partial write requests into the retrieved first cache line.

23. The method of claim 22, further comprising merging a second of the plurality of partial write requests into the retrieved first cache line if the retrieved first cache line is associated with the second of the plurality of partial write requests.

24. The method of claim 22, further comprising merging the first of the plurality of partial write requests into the first cache line if the first cache line is stored in the write cache storage.

25. A machine-readable medium having stored thereon instructions, which when executed by a processor cause said processor to perform:

receiving a plurality of partial write requests for merging into associated cache lines of write data in write cache storage;

determining if a first cache line associated with a first of the plurality of partial write requests is stored in the write cache storage; and

if the first cache line is not stored in the write cache storage:

retrieving the first cache line from memory;

storing the retrieved first cache line in the write cache storage; and

merging the first of the plurality of partial write requests into the retrieved first cache line.

26. The medium of claim 25, further comprising merging a second of the plurality of partial write requests into the retrieved first cache line if the retrieved first cache line is associated with the second of the plurality of partial write requests.

27. The medium of claim 25, further comprising merging the first of the plurality of partial write requests into the first cache line if the first cache line is stored in the write cache storage.

28. An apparatus, comprising:

write cache storage to receive write requests and to store cache lines of write data;

a flush dispatcher coupled to the write cache storage to dispatch the cache lines to memory;

control logic to:

select a first cache line with a first address in the write cache storage for dispatching;

dispatch the first cache line to memory if the number of cache lines in the write cache storage exceeds a first predetermined value;

not dispatch any of the cache lines to memory if the number of cache lines in the write cache storage does not exceed the first predetermined value;

determine if a second cache line in the write cache storage has a second address within a predetermined range of the first address;

dispatch the second cache line if the second address is within the predetermined range of the first address;

determine if a third cache line associated with a particular one of a plurality of partial write requests is stored in the write cache storage;

if the third cache line is not stored in the write cache storage:

retrieve the third cache line from memory;

store the retrieved third cache line in the write cache storage; and

merge the particular one of the plurality of partial write requests into the retrieved third cache line.

29. The apparatus of claim 28, wherein the predetermined range is programmable.

30. The apparatus of claim 28, wherein the control logic is further to:

dispatch the first cache line with a high priority if the number of cache lines in the write cache storage exceeds a second predetermined value higher than the first predetermined value; and

dispatch the first cache line with a low priority if the number of cache lines in the write cache storage exceeds the first predetermined value and does not exceed the second predetermined value.